

# Overview of Networking Devices

2.1.

- (a) Number of channels=  $12 \times 5 \times 10 = 600$
- (b) Capacity=  $600 \times 4 \text{ KHZ} = 2.4 \text{ MHZ}$

2.2. Total output bit-rate of the multiplexer is 160 Kb/s

- (a) Total bit-rate from analog links  
 $= (5 \text{ KHz} + 2 \text{ KHz} + 1 \text{ KHz}) \times 2 \text{ samples/cycle} \times 5 \text{ bits/sample}$   
 $= 80 \text{ Kb/s}$

- (b) Total bit-rate from digital links =  $160 \text{ Kb/s} - 80 \text{ Kb/s} = 80 \text{ Kb/s}$   
 Total bit-rate per digital line =  $\frac{80 \text{ Kb/s}}{4 \text{ lines}} = 20 \text{ Kb/s}$

Pulse stuffing per digital line =  $20 \text{ Kb/s} - 8 \text{ Kb/s} = 12 \text{ Kb/s}$

- (c) For a fair share assignment, the size of channels formed on the frame is proportional to the data rate of that line. Assuming 5-b increments in the length of each channel, we need a total of 3 variable-length channels (10 b + 25 b + 5 b) for the three analog lines, four channels of 10 b long each for the four digital lines, plus a 5 b control channel and a guard bit.

Therefore, the frame size =  $10 + 25 + 5(\text{analog}) + 4 \times 10(\text{digital}) + 5(\text{control}) + 1(\text{guard}) = 86 \text{ b}$

$$\text{Frame rate} = \frac{160 \times 10^3 \text{ b/s}}{86 \text{ b/frame}} = 1,860 \text{ frames/s}$$


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2.3.

(a) Number of characters are = 1 (sync) + 99 (data) = 100

$$\text{Synchronization bit rate} = \frac{4800 \text{ b/s}}{100} \approx 50 \text{ b/s}$$

Number of 150 b/s terminals

$$= \frac{4800 - (2 \times 600 + 5 \times 300 + 50) \text{ b/s}}{150 \text{ b/s}} = 13.6 \approx 13 \text{ terminals}$$

(b) The number of characters for synchronization is proportional to bit rates. For example, since we need 12 characters for 150 b/s terminals, therefore we need 3 characters for synchronization. Frame format in terms of bits is:

$$\begin{aligned} & 2 \times (12 \text{ char} \times 10 \text{ b/char}) + 5 \times (6 \text{ char} \times 10 \text{ b/char}) + 13 \times (3 \text{ char} \times 10 \text{ b/char}) + \\ & 3 \times 10 \text{ b/char} + 1 \times 10 \text{ b/char} \\ & = 970 \text{ b/frame} \end{aligned}$$


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2.4.

(a) #bits/frame (total) =  $2 \text{ Mb/s} \times 26 \mu\text{s/frame} = 52 \text{ bits/frame}$

$$\text{\#bits/frame (data)} = 52 \text{ bits/frame} - 10 = 42 \text{ bits/frame}$$

$$\text{\#channels} = n = 42 \text{ bits/frame} \frac{1}{6 \text{ bits/ch}} = 7 \text{ ch/frame}$$

(b)  $P[\text{clipping}] = \sum_{i=n}^{m-1} \binom{m-i}{i} p^i (1-p)^{m-i-1}$

$$m = 10, n = 7, p = 0.9$$

$$P[\text{clipping}] = 0.947$$

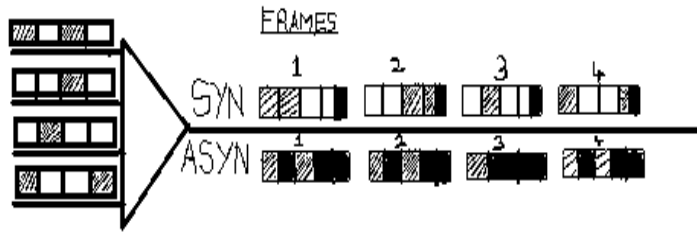

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2.5. N/A

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2.6.

(a)



(b) Mux Output Rate  
 = 4 lines \* 10 Mb/s = 40 Mb/s

Frame Size =  
 (For Synchronous TDM): 5 ch/frames \* 4 b/ch = 20 b/frames  
 (For asynchronous TDM): Ave: (20+20+12+20)/4 = 18 b/frames

Frame Rate =  
 (For Synchronous TDM): 40 Mb/s / 20 b/frame = 2 Mframes/s  
 (For asynchronous TDM): 40 Mb/s / 18 b/frame = 2.22 Mframes/s

(c) Speed of Clock: (4 lines \* 10 Mb/s) \* 1 cycle/b  
 = 40 M cycles/b  
 = 40 MHz

2.7.

(a)  $\rho = \frac{t_a}{t_c + d} = 2/8 = 25\%$

(b) 
$$P_{j=3} = \frac{\binom{m}{j} \left(\frac{t_i}{t_a}\right)^j}{\sum_{i=0}^j \binom{m}{j} \left(\frac{t_a}{t_d}\right)^i} = \frac{\binom{8}{3} \left(\frac{2}{6}\right)^3}{\sum_{j=0}^3 \binom{8}{1} \left(\frac{2}{6}\right)^i} \approx 21\%$$

(c) 
$$B = P_{j=n=4} = \frac{\binom{m}{n} (1/3)^n}{\sum_{i=0}^n \binom{m}{i} (1/3)^i} = \frac{\binom{8}{7} (1/3)^4}{\sum_{i=0}^4 \binom{8}{i} (1/3)^i}$$
  

$$= \frac{70/81}{1+8/3+28/9+56/27+70/81} \approx 9\%$$

(d)  $E[C] = \sum_{j=1}^4 j p_j = 1(0.275) + 2(0.32) + 3(0.213) + 4(0.0889) \approx 1.94$

2.8.

(a)  $m = 4$

$n = 2$

$$\begin{aligned}\text{Prob}[\text{clipping}] = P_c &= \sum_{i=2}^3 \binom{3}{i} \rho^i (1-\rho)^{3-i} \\ &= 10.4\% \text{ for } \rho = 0.2 \\ &= 35.2\% \text{ for } \rho = 0.4 \\ &= 64.8\% \text{ for } \rho = 0.6 \\ &= 89.6\% \text{ for } \rho = 0.8\end{aligned}$$

(b)  $m = 4$

$n = 3$

$$\begin{aligned}\text{Prob}[\text{clipping}] P_c &= \sum_{i=3}^3 \binom{3}{3} \rho^3 (1-\rho)^{3-3} \\ &= 0.0\% \text{ for } \rho = 0.2 \\ &= 6.4\% \text{ for } \rho = 0.4 \\ &= 21.6\% \text{ for } \rho = 0.6 \\ &= 51.2\% \text{ for } \rho = 0.8\end{aligned}$$

(c)  $n = 4$

$P_4 = 100\%$

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2.9.

$$\rho = \frac{t_a}{t_a + t_d} = 0.9$$

for  $m = 11$  and  $n = 10$ :

$P_c$  = the clipping probability

$$= \sum_{i=n}^{m-1} \binom{m-1}{i} \rho^i (1-\rho)^{m-1-i} = \binom{10}{10} \rho^{10} (1-\rho)^0 = \rho^{10} \approx 0.35$$

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2.10.

$$\frac{1}{\mu} \left( 1 - \frac{\eta}{\rho} m \right)$$

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2.11. See Figure 2.1.

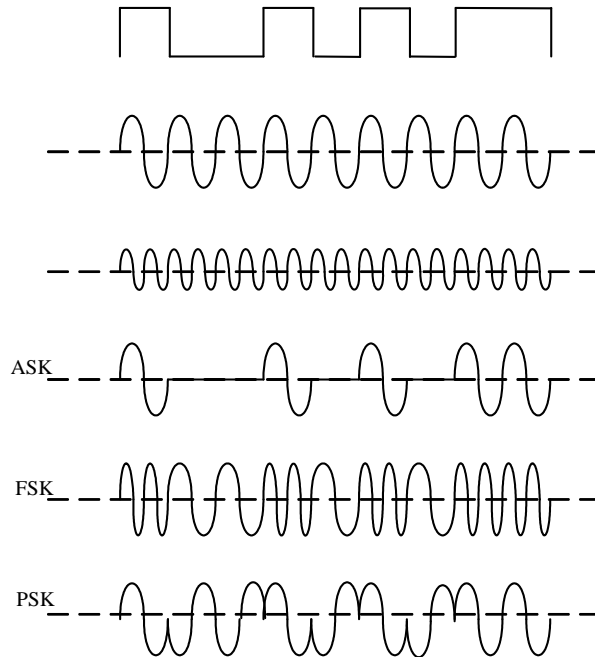


FIGURE 2.1 Modulation techniques in exercise 2.11

2.12.

- (a) Assume a packet incoming at input port of IPP has length of L bits. Then,

$$T = \frac{d + 50}{r} \Rightarrow \frac{\partial T^2}{\partial d \partial r} = 0 \Rightarrow d_{\text{opt}}, r_{\text{opt}}$$

Therefore ways to optimize the transmission delay T are followings:

- Increase transmission rate (r) by reducing clock cycle time of CPU.
- Define value of d to be equal to highest-probability packet length(L).

- (b) For example, if the switch fabric has 5 stages of routing in its internal network, the processing delay mostly depends on AND gate switch time of gates on a fabric. Assume applying CMOS transistors, which are slowest technology for switching transistors, for this switch fabric. Assuming 50-80 ns switch time for CMOS AND gate, the total propagation delay in this switch fabric = 80 ns × 5 stages = 0.4 μs. On the other hand, the delay in IPP (D) mostly depends on packet fragmentation and encapsulation delay time. Typical value of this delay time is about tens or hundreds of milliseconds for a 512-bytes packet.

Therefore processing delay in the switch fabric is not significant compared to delay in IPP.